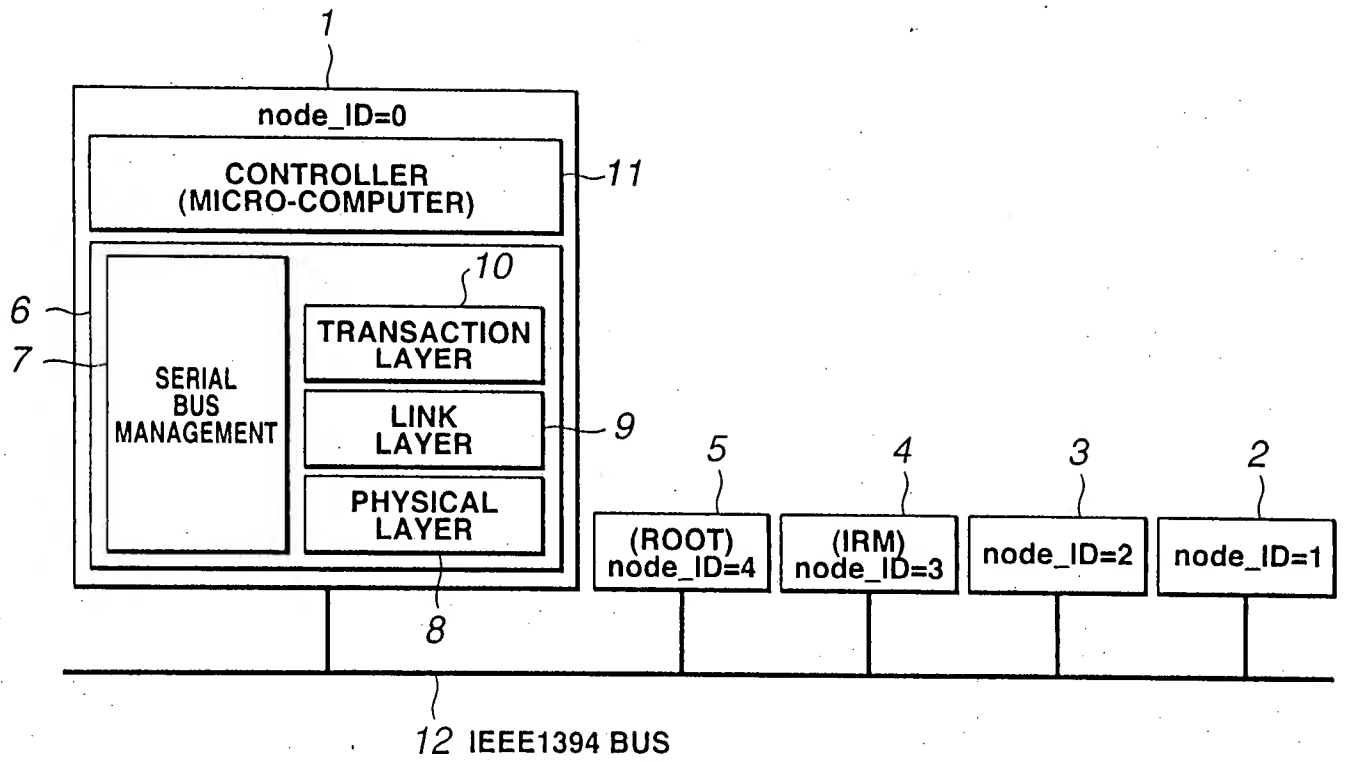

1
node_ID=0
CONTROLLER
(MICRO-COMPUTER)
11
10
6
7
SERIAL
BUS
MANAGEMENT
TRANSACTION
LAYER
LINK
LAYER
9
PHYSICAL
LAYER
8
5
4
3
2
(ROOT)
node_ID=4
(IRM)
node_ID=3
node_ID=2
node_ID=1
12 IEEE1394 BUS

FIG.1

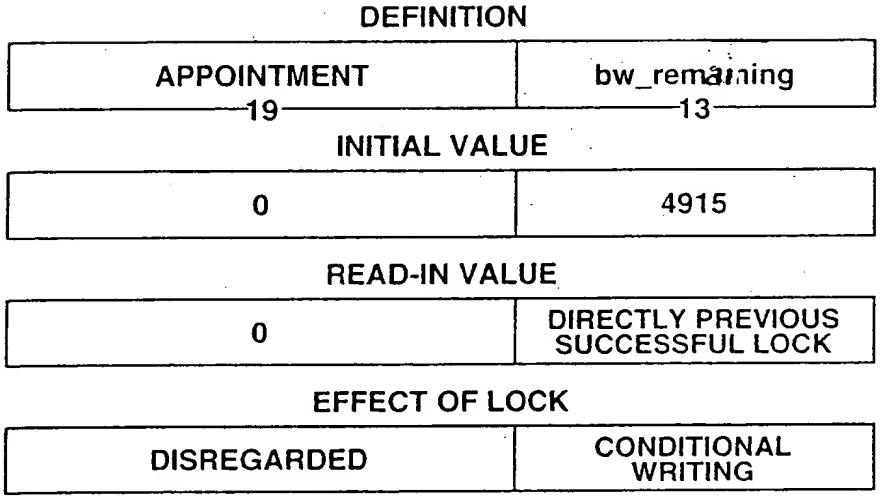

DEFINITION
APPOINTMENT
bw_remaining
19
13
INITIAL VALUE
0
4915
READ-IN VALUE
0
DIRECTLY PREVIOUS SUCCESSFUL LOCK
EFFECT OF LOCK
DISREGARDED
CONDITIONAL WRITING

FIG.2

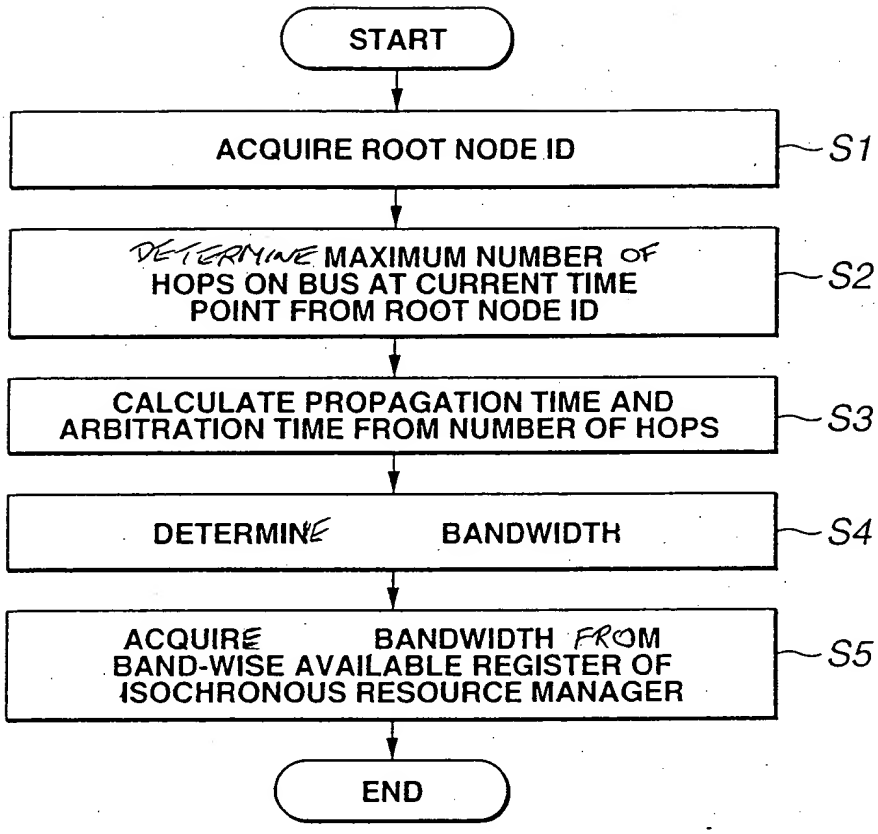

START
ACQUIRE ROOT NODE ID
S1
DETERMINE MAXIMUM NUMBER OF HOPS ON BUS AT CURRENT TIME POINT FROM ROOT NODE ID
S2
CALCULATE PROPAGATION TIME AND ARBITRATION TIME FROM NUMBER OF HOPS
S3
DETERMINE BANDWIDTH
S4
ACQUIRE BANDWIDTH FROM BAND-WISE AVAILABLE REGISTER OF ISOCHRONOUS RESOURCE MANAGER
S5
END

FIG.3

FIG.4A

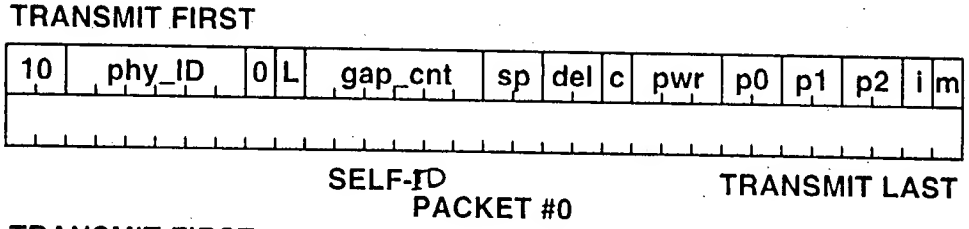
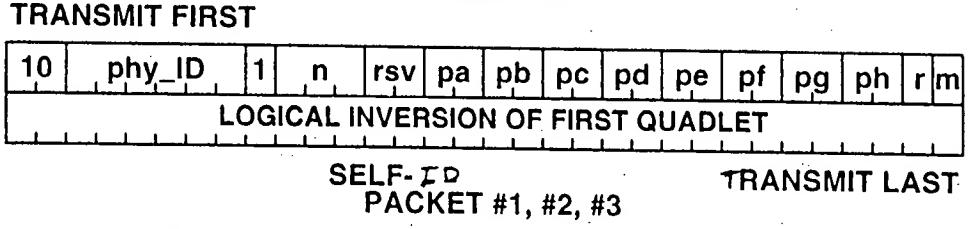


FIG.4B



	n	pa	pb	pc	pd	pe	pf	pg	ph
PACKET #1	0	p3	p4	p5	p6	p7	p8	p9	p10
PACKET #2	1	p11	p12	P13	p14	p15	p16	p17	p18
PACKET #3	2	p19	p20	p21	p22	p23	p24	p25	p26

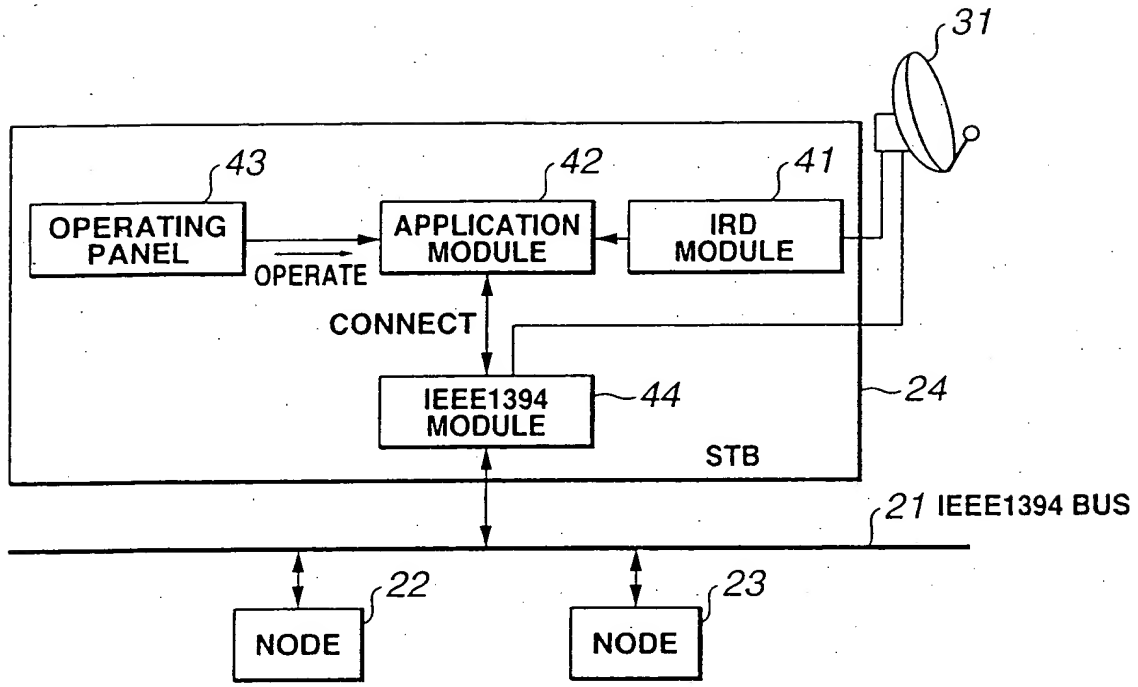

31
43
42
41
OPERATING PANEL
APPLICATION MODULE
IRD MODULE
OPERATE
CONNECT
IEEE1394 MODULE
44
24
STB
21 IEEE1394 BUS
22
23
NODE
NODE

FIG.5

FIG. 6

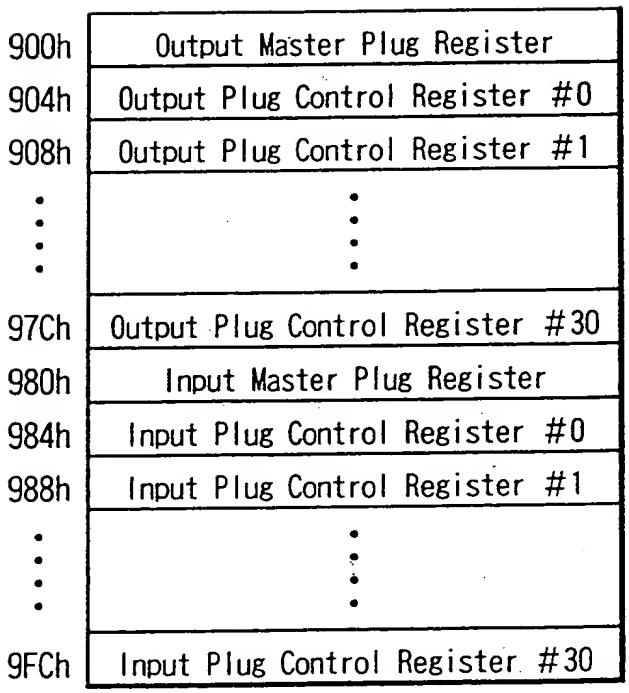

900h
Output Master Plug Register
904h
Output Plug Control Register #0
908h
Output Plug Control Register #1
97Ch
Output Plug Control Register #30
980h
Input Master Plug Register
984h
Input Plug Control Register #0
988h
Input Plug Control Register #1
9FCh
Input Plug Control Register #30

FIG. 7A

oMPR

data rate capability	broadcast channel base	non-persistent extension field	persistent extension field	reserved	number of output plugs
2	6	8	8	3	5 (bit)

FIG. 7B

oPCR[n]

on-line	broadcast connection counter	point-to-point connection counter	reserved	channel number	data rate	overhead ID	payload
1	1	6	2	6	2	4	10 (bit)

FIG. 7C

iMPR

data rate capability	reserved	non-persistent extension field	persistent extension field	reserved	number of input plugs
2	6	8	8	3	5 (bit)

FIG. 7D

iPCR[n]

on-line	broadcast connection counter	point-to-point connection counter	reserved	channel number	reserved
1	1	6	2	6	16 (bit)

FIG. 8

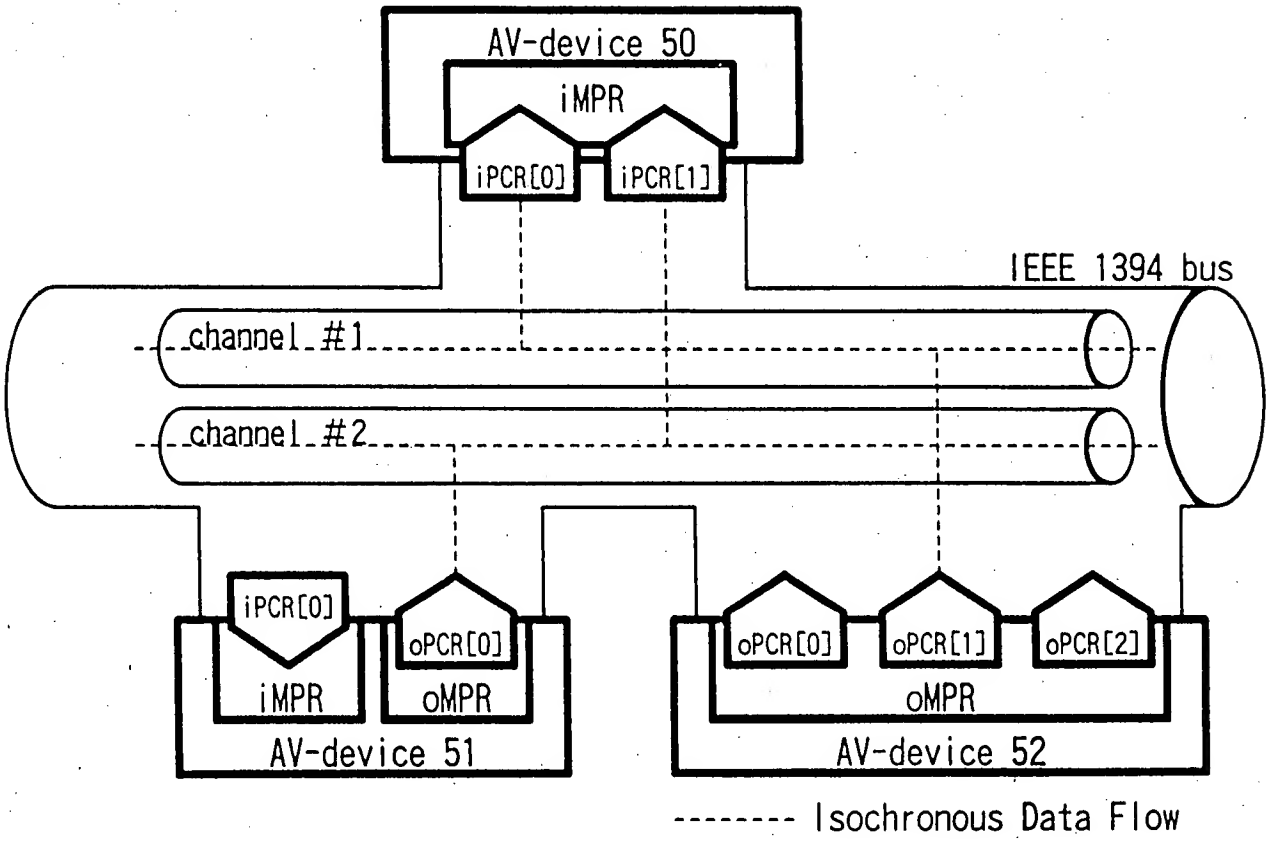

AV-device 50
iMPR
iPCR[0]
iPCR[1]
IEEE 1394 bus
channel #1
channel #2
iPCR[0]
iMPR
oPCR[0]
oMPR
AV-device 51
oPCR[0]
oPCR[1]
oPCR[2]
oMPR
AV-device 52
Isochronous Data Flow

FIG. 9

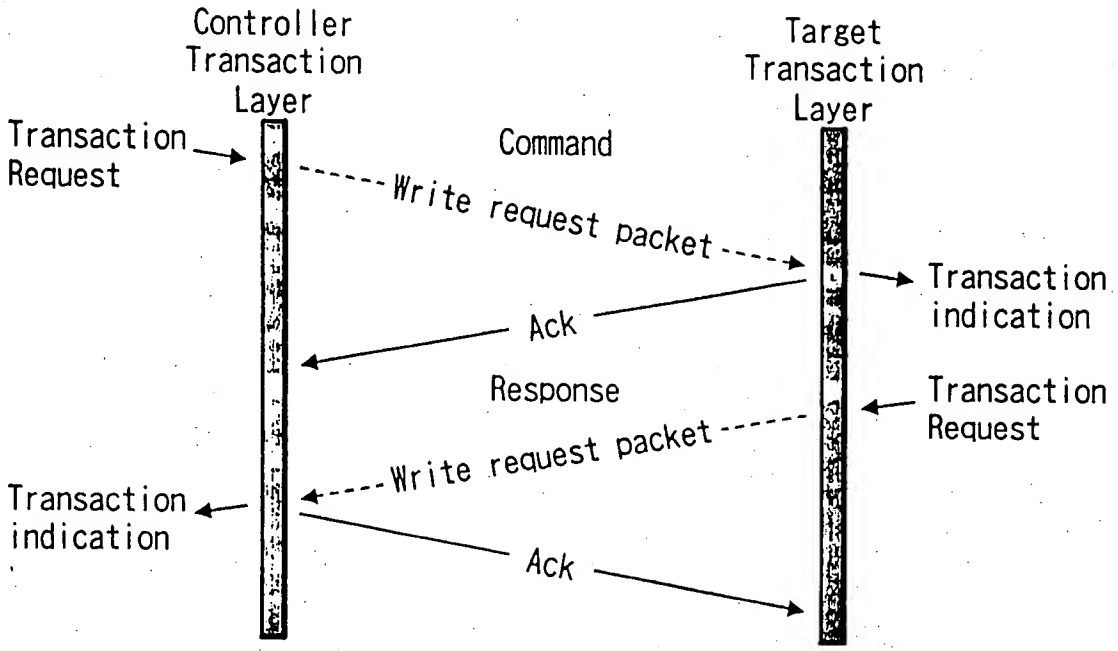

Controller Transaction Layer
Target Transaction Layer
Transaction Request
Command
Write request packet
Transaction indication
Ack
Response
Transaction Request
Write request packet
Transaction indication
Ack

FIG. 10

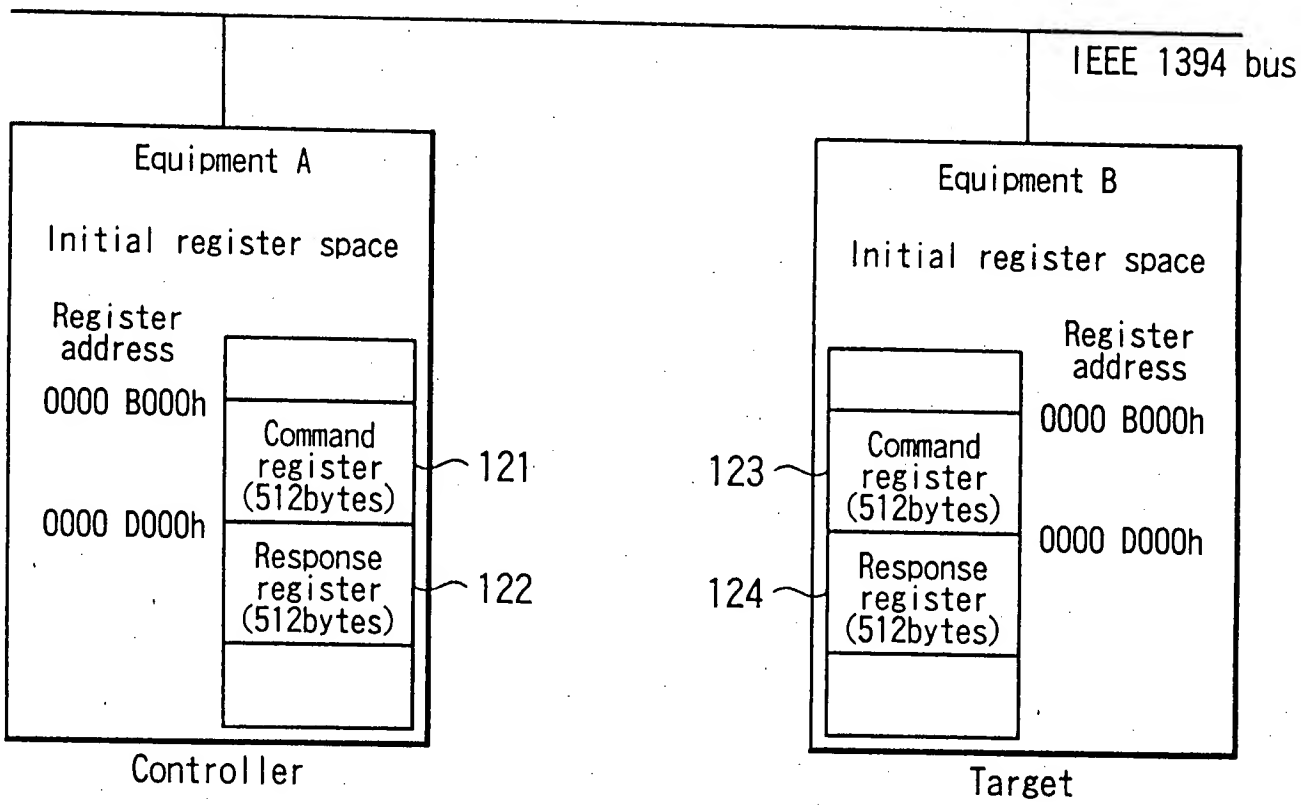

IEEE 1394 bus
Equipment A
Initial register space
Register address
0000 B000h
0000 D000h
Command register (512bytes)
Response register (512bytes)
121
122
Controller
Equipment B
Initial register space
Register address
0000 B000h
0000 D000h
123
124
Command register (512bytes)
Response register (512bytes)
Target

FIG. 11

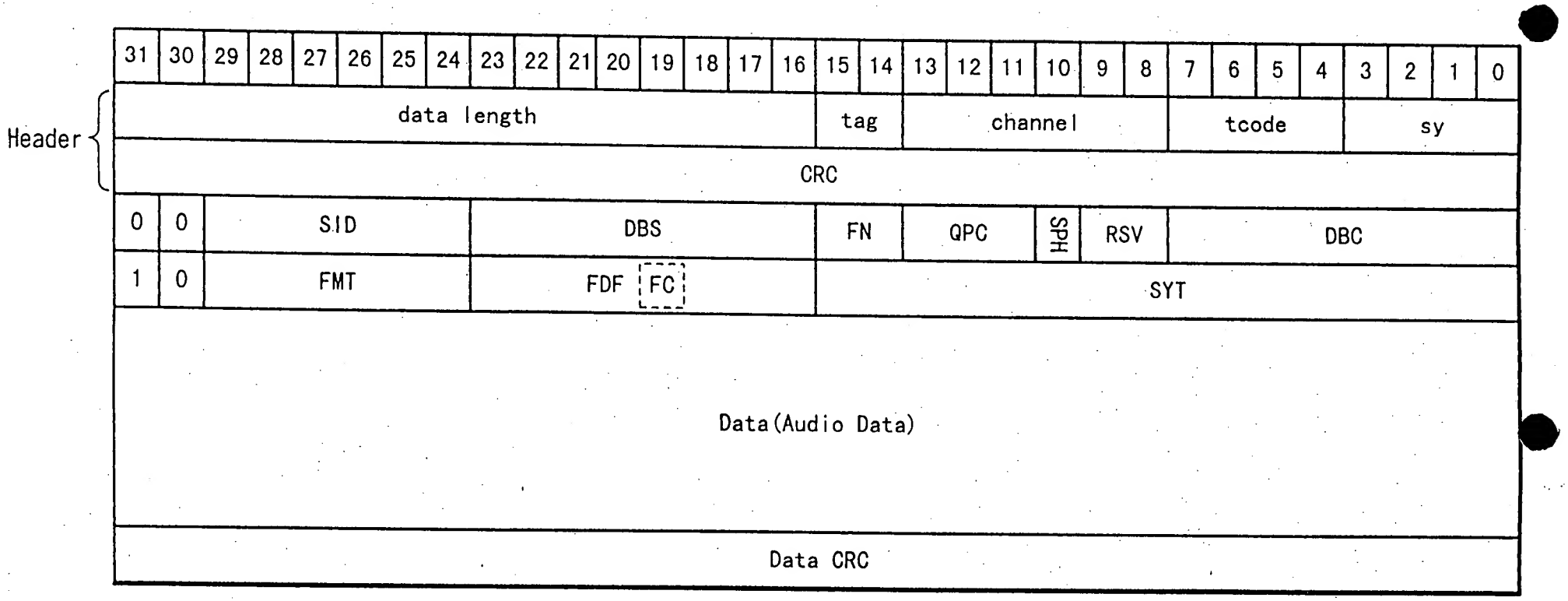
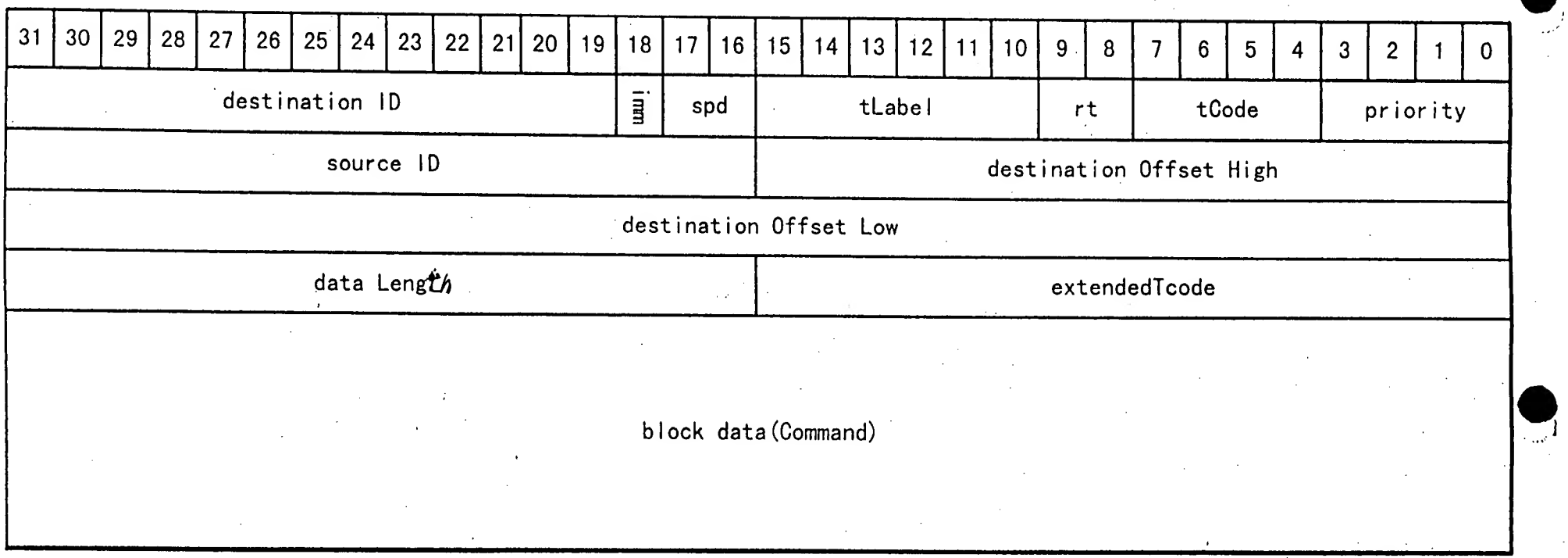

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Header
data length
tag
channel
tcode
sy
CRC
0 0
SID
DBS
FN
QPC
SPH
RSV
DBC
1 0
FMT
FDF
FC
SYT
Data(Audio Data)
Data CRC

FIG. 12


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
destination ID
spd
tLabel
rt
tCode
priority
source ID
destination Offset High
destination Offset Low
data Length
extendedTcode
block data(Command)

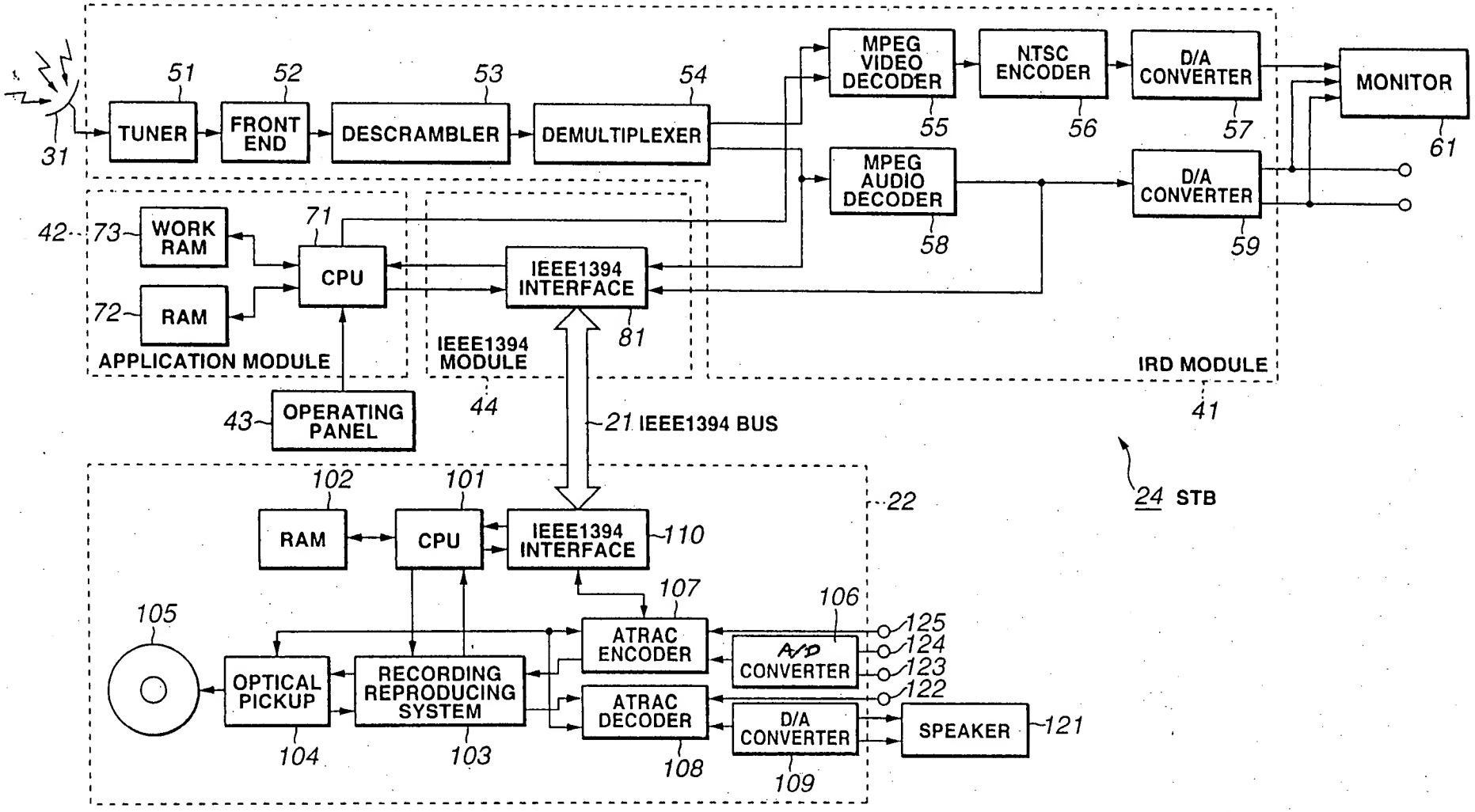

31
TUNER
51
FRONT END
52
DESCRAMBLER
53
DEMULTIPLEXER
54
MPEG VIDEO DECODER
55
NTSC ENCODER
56
D/A CONVERTER
57
MONITOR
61
MPEG AUDIO DECODER
58
D/A CONVERTER
59
42
73
WORK RAM
71
CPU
IEEE1394 INTERFACE
81
72
RAM
APPLICATION MODULE
IEEE1394 MODULE
44
IRD MODULE
41
43
OPERATING PANEL
21 IEEE1394 BUS
24 STB
22
102
RAM
101
CPU
IEEE1394 INTERFACE
110
107
106
105
ATRAC ENCODER
A/D CONVERTER
125
124
123
122
OPTICAL PICKUP
RECORDING REPRODUCING SYSTEM
ATRAC DECODER
D/A CONVERTER
SPEAKER
121
104
103
108
109

FIG. 3

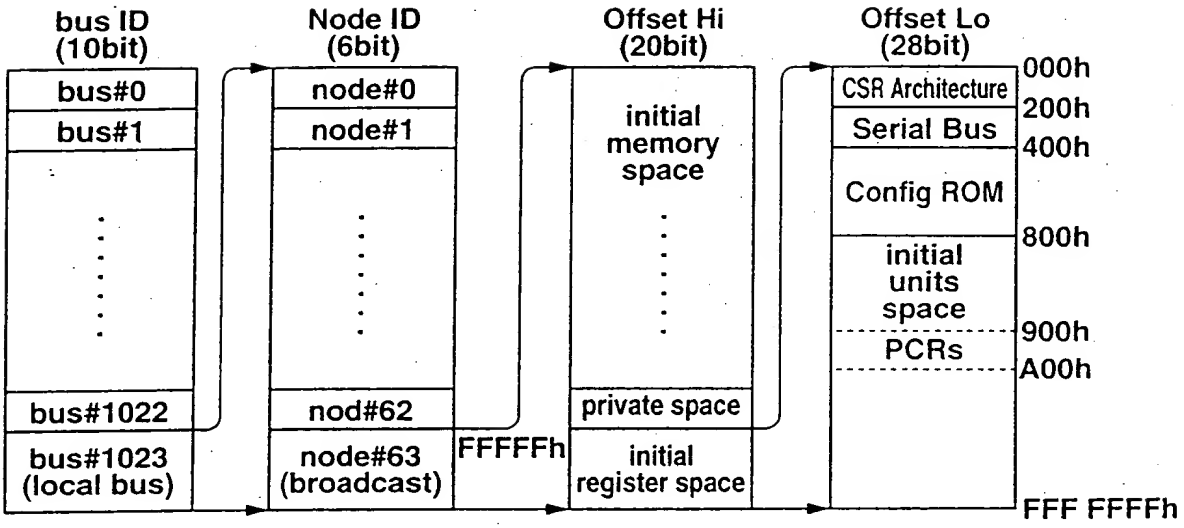

bus ID
(10bit)
Node ID
(6bit)
Offset Hi
(20bit)
Offset Lo
(28bit)
bus#0
bus#1
bus#1022
bus#1023
(local bus)
node#0
node#1
nod#62
node#63
(broadcast)
FFFFFFh
initial
memory
space
private space
initial
register space
CSR Architecture
Serial Bus
Config ROM
initial
units
space
PCRs
000h
200h
400h
800h
900h
A00h
FFF FFFFh

FIG. 14

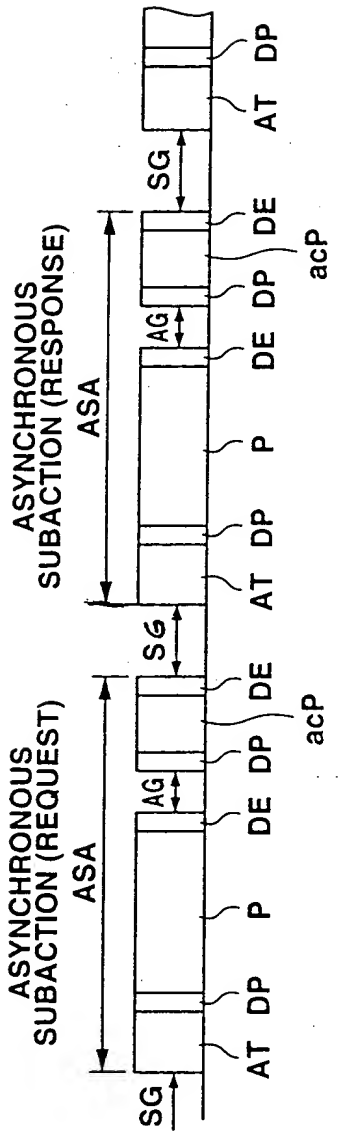

ASYNCHRONOUS SUBACTION (REQUEST)
ASA
SG
AT
DP
P
DE
AG
DP
acP
DE
SG
ASYNCHRONOUS SUBACTION (RESPONSE)
ASA
AT
DP
P
DE
AG
DP
acP
DE
SG
AT
DP

FIG. 15

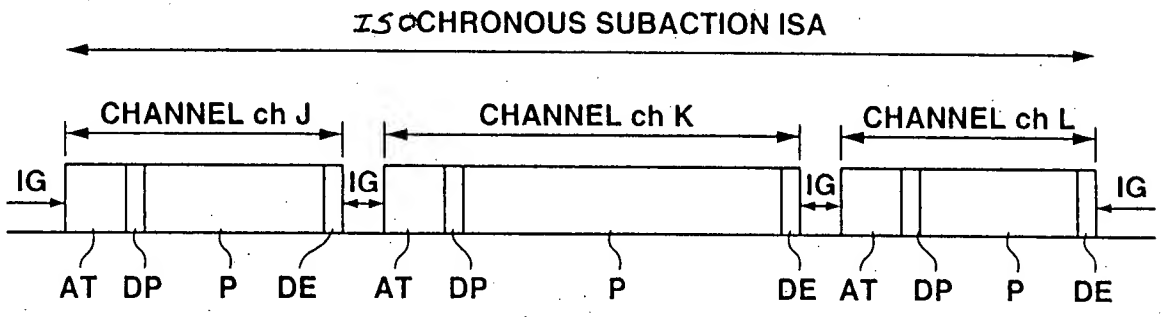

ISOCHRONOUS SUBACTION ISA
CHANNEL ch J
CHANNEL ch K
CHANNEL ch L
IG
IG
IG
IG
AT
DP
P
DE
AT
DP
P
DE
AT
DP
P
DE

FIG. 16

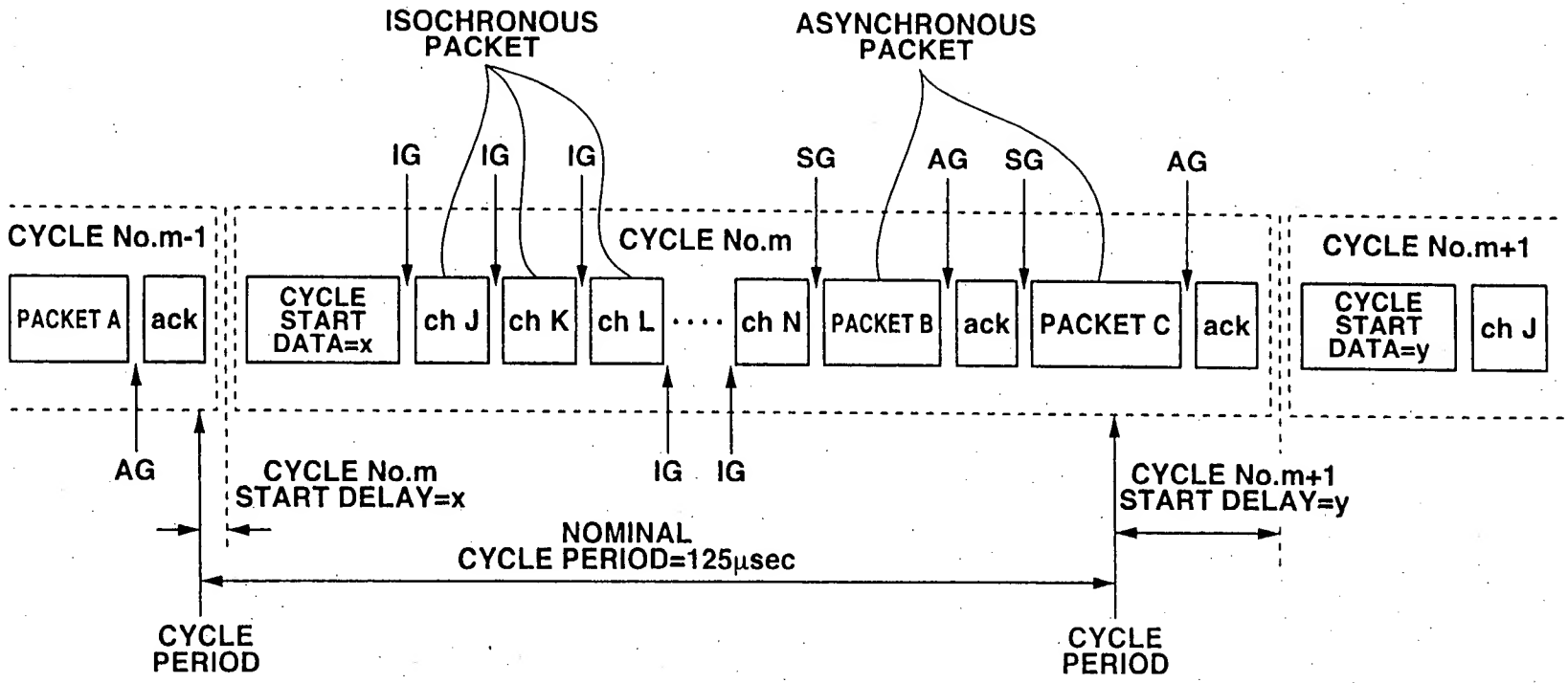

ISOCHRONOUS PACKET
ASYNCHRONOUS PACKET
IG
IG
IG
SG
AG
SG
AG
CYCLE No.m-1
CYCLE No.m
CYCLE No.m+1
PACKET A
ack
CYCLE START DATA=x
ch J
ch K
ch L
ch N
PACKET B
ack
PACKET C
ack
CYCLE START DATA=y
ch J
AG
CYCLE No.m START DELAY=x
IG
IG
CYCLE No.m+1 START DELAY=y
NOMINAL CYCLE PERIOD=125μsec
CYCLE PERIOD
CYCLE PERIOD

FIG.17

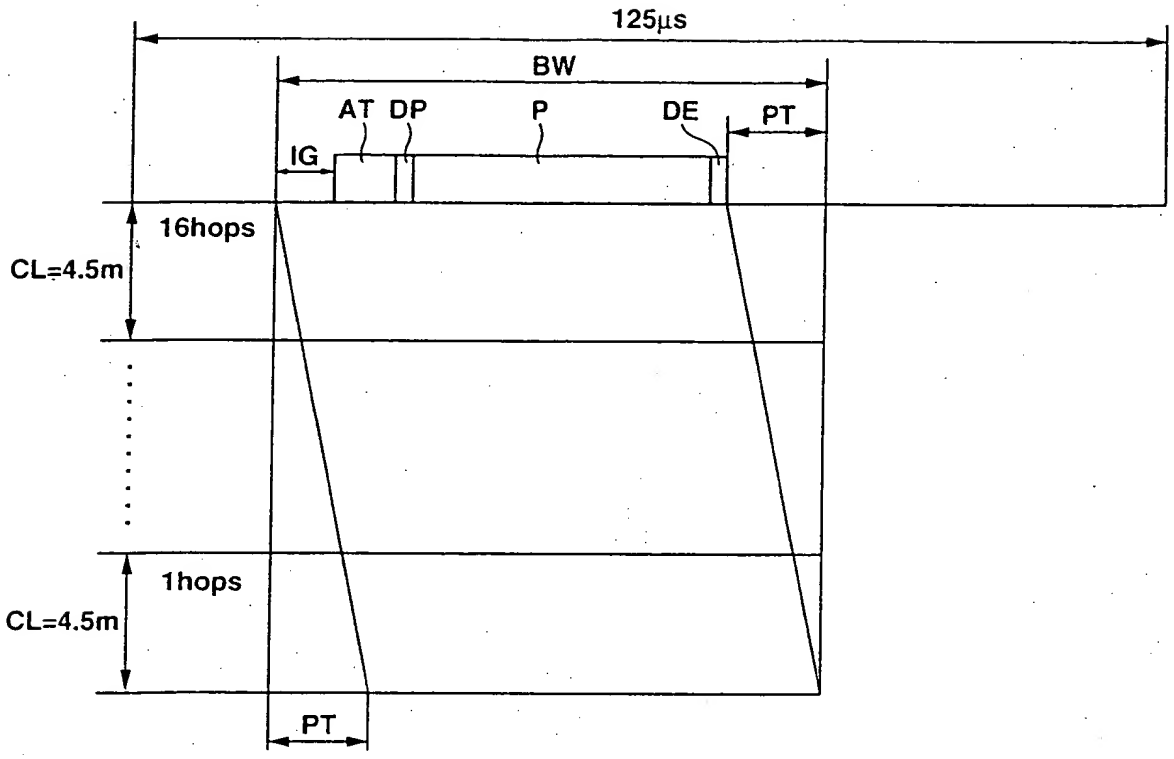


FIG.18

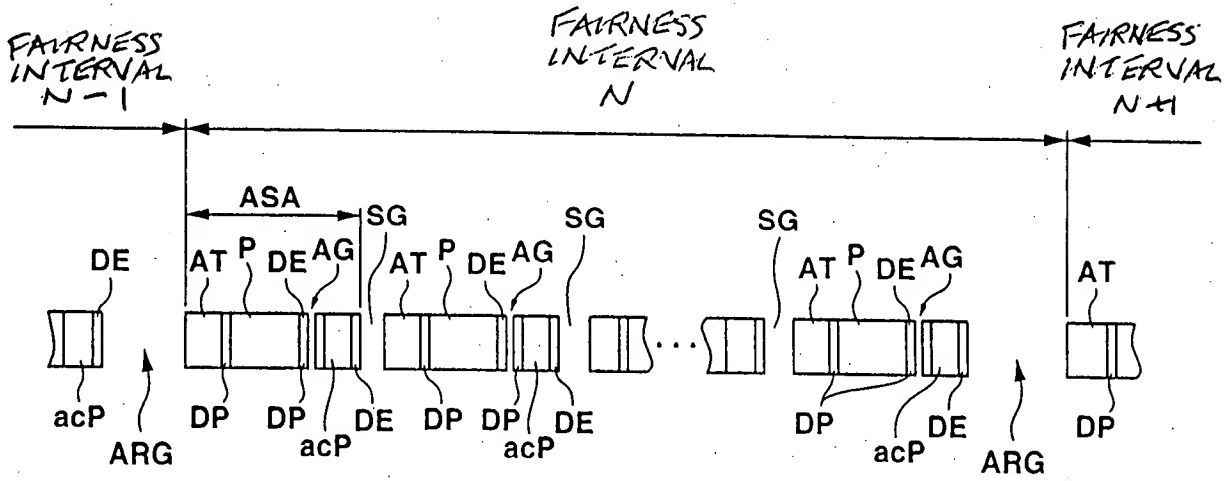

FAIRNESS INTERVAL N-1
FAIRNESS INTERVAL N
FAIRNESS INTERVAL N+1
ASA
SG
SG
SG
DE
AT P DE AG
AT P DE AG
AT P DE AG
AT
acP
ARG
DP DP
acP
DE
DP DP
acP
DE
DP
acP
DE
ARG
DP

FIG.19